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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: :
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Chong Min KYUNG et al. :
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Serial No: 09/760,645 :
 :
Filed: January 17, 2001 :
 :
For: APPARATUS AND METHOD FOR VERIFYING :
A LOGIC FUNCTION OF A SEMICONDUCTOR)
CHIP :

Examiner: Unassigned
Group Art Unit: 2123

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DEC 10 2002

Technology Center 2100

Assistant Commissioner of Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to Rule 37 C.F.R. §1.51(b), §1.56, §1.97, and §1.98, this Information Disclosure Statement is submitted in the above-identified patent application. A listing of documents to be published on the face of any patent granted from this application is submitted herewith on Form PTO-1449. Any other documents or information submitted for consideration by the Examiner are listed in this paper. A copy of each U.S. and foreign patent, or each publication or portion thereof listed or herein identified is submitted herewith, except that a copy of any U.S. patent application identified herein or any patent, publication or other information listed herein cited or submitted in a prior application relied upon for an earlier filing date under 35 U.S.C. §120 and identified below, is not submitted herewith.



Serial No. 09/760,645
Group Art Unit: 2123

This Information Disclosure Statement is submitted prior to the mailing date of the first Office Action on the merits received by Applicant in the above-identified application.

The Examiner is requested to acknowledge consideration of the information provided in this paper in accordance with prescribed procedures.

Respectfully submitted,

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Date: December 9, 2002

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